

IN THE CLAIMS

What is claimed is:

1. 1. A method of forming a microelectronic structure comprising:
 2. providing a substrate comprising source/drain and gate regions, wherein the gate region comprises a metal layer disposed on a gate dielectric layer, and
 5. laser annealing the substrate.
1. 2. The method of claim 1 wherein providing a substrate comprising source/drain and gate regions, wherein the gate region comprises a metal layer disposed on a gate dielectric layer comprises providing a substrate comprising source/drain and gate regions, wherein the gate region comprises a metal layer comprising a work function from about 3.9 electron volts to about 5.2 electron volts that is disposed on the gate dielectric layer.
1. 3. The method of claim 1 wherein providing a substrate comprising source/drain and gate regions, wherein the gate region comprises a metal layer disposed on a gate dielectric layer further comprises wherein the metal layer does not substantially diffuse into the gate dielectric layer.

1 4. The method of claim 1 wherein providing a substrate comprising
2 source/drain and gate regions, wherein the gate region comprises a metal
3 layer disposed on a gate dielectric layer further comprises wherein the metal
4 layer does not substantially diffuse into a polysilicon layer disposed on the
5 metal layer.

1 5. The method of claim 1 wherein laser annealing the substrate.
2 comprises exposing the substrate to a laser beam for a time sufficient to
3 activate an implanted species.

1 6. The method of claim 1 wherein laser annealing the substrate
2 comprises exposing the substrate to a laser beam pulsed at about 20
3 nanosecond intervals or less.

1 7. The method of claim 1 wherein laser annealing the substrate
2 comprises activating an implanted species in the source/drain regions by
3 laser annealing.

1 8. The method of claim 7 wherein activating an implanted species in the
2 source/drain regions by laser annealing comprises activating an implanted
3 species in the source/drain regions, wherein the ratio of the depth of the

4 source/drain regions to the length of the source/drain regions is less than
5 about 1:2 by laser annealing.

1 9. The method of claim 1 wherein providing a substrate comprising
2 source/drain and gate regions, wherein the gate region comprises a metal
3 layer disposed on a gate dielectric layer comprises providing a substrate
4 comprising source/drain and gate regions, wherein the gate region comprises
5 a metal layer disposed on a high k dielectric layer.

1 10. The method of claim 1 wherein providing a substrate comprising
2 source/drain and gate regions, wherein the gate region comprises a metal
3 layer comprises providing a substrate comprising source/drain and gate
4 regions, wherein the gate region comprises a metal layer selected from the
5 group consisting of tungsten, platinum, ruthenium, palladium, molybdenum
6 and niobium, and their alloys, metal carbides, metal nitrides, metal carbides
7 and conductive metal oxides.

1 11. A method of forming a microelectronic structure comprising;
2 providing a substrate comprising doped source/drain and gate
3 regions, wherein the gate region comprises a metal layer disposed on
4 a high k dielectric layer, and wherein the metal layer comprises a work

5 function approximately equal to a work function of n doped polysilicon;
6 and
7 forming shallow source/drain regions by laser annealing the
8 substrate.

1 12. The method of claim 11 wherein forming shallow source/drain regions
2 comprises forming source/drain regions wherein the ratio of the depth of the
3 source/drain regions to the length of the source/drain regions is less than
4 about 1:2.

1 13. The method of claim 11 wherein providing a substrate comprising
2 doped source/drain and gate regions, wherein the gate region comprises a
3 metal layer disposed on a high k dielectric layer, and wherein the metal layer
4 comprises a work function approximately equal to a work function of n doped
5 polysilicon comprises providing a substrate comprising doped source/drain
6 and gate regions, wherein the gate region comprises a metal layer disposed
7 on a high k dielectric layer, and wherein the metal layer comprises a work
8 function from about 3.9 to about 4.2 electron volts.

1 14. The method of claim 11 wherein providing a substrate comprising
2 doped source/drain and gate regions, wherein the gate region comprises a
3 metal layer disposed on a high k dielectric layer, and wherein the metal layer

4 comprises a work function approximately equal to a work function of n doped
5 polysilicon comprises providing a substrate comprising doped source/drain
6 and gate regions, wherein the gate region comprises a metal layer disposed
7 on a high k dielectric layer, and wherein the metal layer comprises a work
8 function approximately equal to a work function of p doped polysilicon.

1 15. The method of claim 11 wherein providing a substrate comprising
2 doped source/drain and gate regions, wherein the gate region comprises a
3 metal layer disposed on a high k dielectric layer, and wherein the metal layer
4 comprises a work function approximately equal to a work function of p doped
5 polysilicon comprises providing a substrate comprising doped source/drain
6 and gate regions, wherein the gate region comprises a metal layer disposed
7 on a high k dielectric layer, and wherein the metal layer comprises a work
8 function comprises a work function from about 4.8 to about 5.1 electron volts.

1 16. The method of claim 11 wherein providing a substrate comprising
2 doped source/drain and gate regions, wherein the gate region comprises a
3 metal layer disposed on a high k dielectric layer comprises providing a
4 substrate comprising doped source/drain and gate regions, wherein the gate
5 region comprises a metal layer disposed on a high k dielectric layer selected
6 from the group consisting of hafnium oxide, zirconium oxide, titanium oxide,
7 and aluminum oxide and /or combinations thereof.

1 17. A structure comprising:

2 a substrate comprising source/drain and gate regions, wherein the

3 gate region comprises a metal layer disposed on a gate dielectric layer,

4 wherein the ratio of the depth of the source/drain regions to the length of the

5 source/drain regions is less than about 1:2, and wherein the metal layer is

6 not substantially diffused into the gate dielectric layer.

1 18. The structure of claim 17 further comprising wherein the metal layer is

2 not substantially diffused into a polysilicon layer disposed on the metal layer.

1 19. The structure of claim 17 wherein the metal layer comprises a work

2 function between about 3.9 and about 4.2 electron volts.

1 20. The structure of claim 17 wherein the metal layer comprises a work

2 function between about 4.8 and about 5.2 electron volts.

1 21. The structure of claim 17 wherein the high k dielectric layer is selected

2 from the group consisting of hafnium oxide, zirconium oxide, titanium oxide,

3 and aluminum oxide and /or combinations thereof.

1 22. The structure of claim 17 wherein the metal layer does not comprise
2 an inter-metallic layer.

1 23. The structure of claim 17 wherein the metal layer comprises a material
2 selected from the group consisting of tungsten, platinum, ruthenium,
3 palladium, molybdenum and niobium, and their alloys, metal carbides, metal
4 nitrides, and conductive metal oxides.

1 24. The structure of claim 17 wherein the metal layer does not comprise a
2 phase changed metal layer.